

Advanced Triggering and Synchronization with PXI

Background – PXI is an increasingly popular form factor for instrumentation and automation in industrial and military applications. This is due to its mechanical ruggedness resulting from adherence to the Compact PCI/Eurocard standard, and low cost from leveraging desktop PCI electrical specifications. In addition, PXI defines several special electrical interfaces to enhance multi-board system design:

- The Trigger Bus is a group of eight lines which are bussed to each slot in a PXI bus segment (group of eight slots). These lines can carry TTL signals such as triggers or clocks.
- The Star Triggers are a group of thirteen bi-directional lines connecting Slot 2 with each of the thirteen possible peripheral slots in the primary and secondary bus

segments. From the Star Trigger Controller slot, low skew TTL triggers can be supplied or received from any peripheral board in the system.

- The Local Busses consist of two groups of thirteen bidirectional lines which connect each peripheral slot with its right and left neighbor. The right and left busses are independent. These lines can carry TTL or analog signals.
- A 10 MHz synchronizing clock is provided by the backplane to all slots.

Additionally, PXI provides an electrical identifier so that each board can identify its slot number. For more information, please see the PXI specifications, which are available at the PXI System Alliance web site (www.pxisa.org).

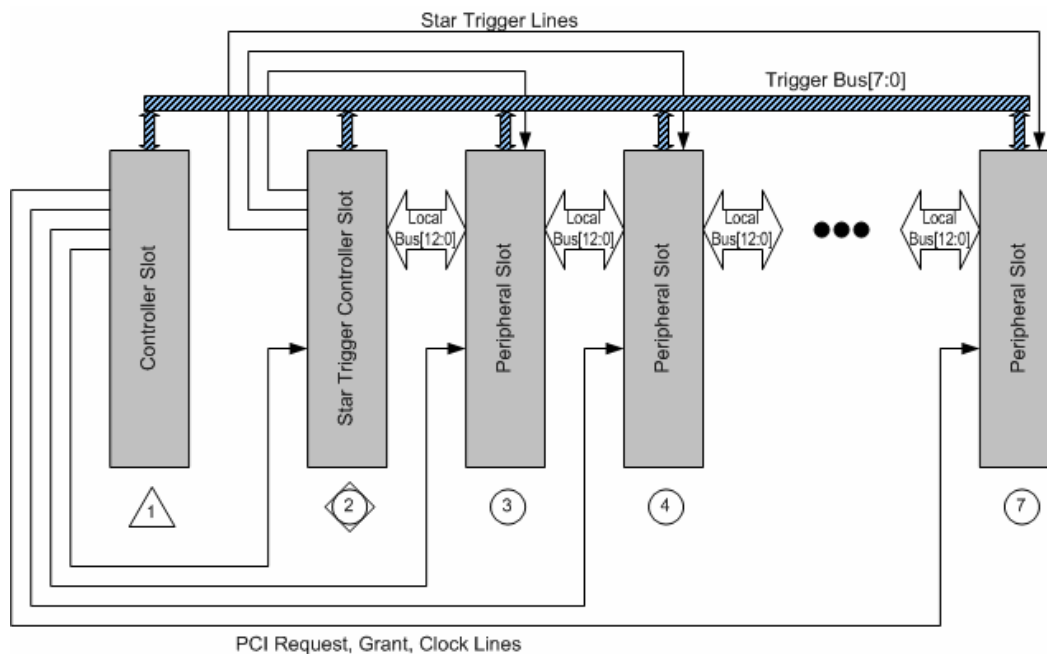


Figure 1 – PXI Electrical Interfaces

Implementation – On the Exacq Technologies XH and XM boards, a subset of the PXI features have been utilized. All Exacq boards in peripheral slots support the Star Trigger as an input trigger. Exacq boards in the Star Trigger Controller Slot (Slot 2) can, via software, re-purpose digital I/O lines as

Star Trigger outputs. A mechanism can be set up, via the ExacqDA SDK API, to allow a board in the Slot 2 to issue star triggers to any or all peripheral slots upon receipt of any trigger by the Slot 2 board. In this way, multiple boards can be triggered to capture

inputs almost simultaneously. This architecture is shown conceptually in Fig 2a.

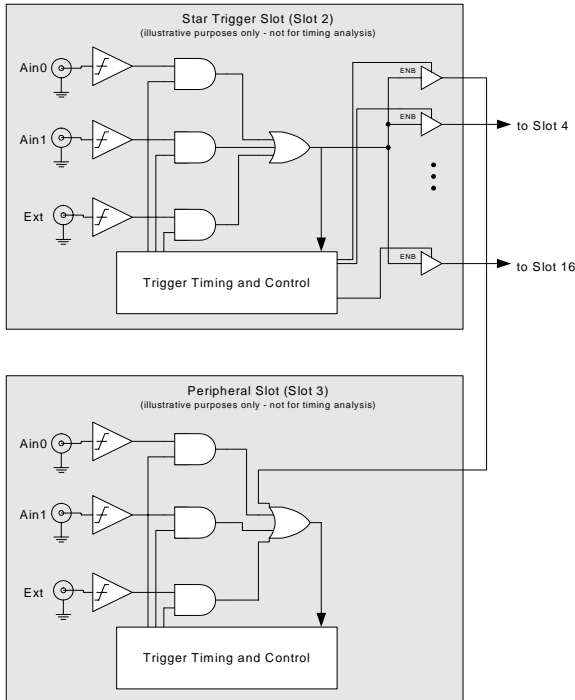


Figure 2a – XH Star Trigger Architecture

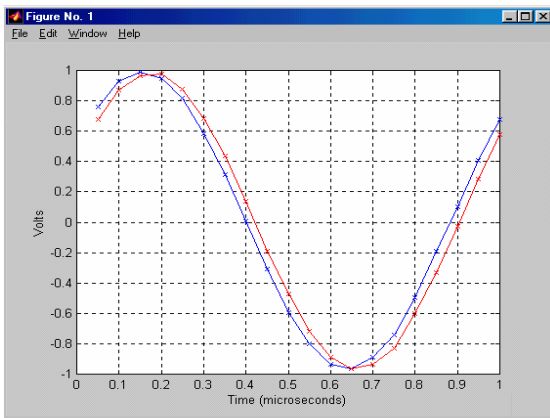


Figure 2b – XH Star Trigger Capture

Figure 2b shows the resulting captured data with the same input applied to two boards. Note the sample time difference of < 20 ns.

The same mechanism facilitates generation of simultaneous outputs across multiple boards. For example, if the output from an XH board in Slot 2 is started via a software trigger, it can simultaneously trigger an output on an XH board in Slot 3 via the star trigger. If the outputs of both boards were started using sequential writes across the PCI bus, there would be at least 100 ns of delay since each

write takes at least 4 PCI bus clocks to complete. This could be 2.5 samples at the peak output rate of 40 MHz on the XH. Worse yet, another PCI bus master could take control of the bus between writes, or the operating system could task switch between calls to consecutive boards, making the delay much longer.

XH boards are capable of driving or receiving external clock on either the auxiliary BNC connector or on the Trigger Bus[7] line. XH boards with DI/O expansion also support a two-wire serial bus on the Local Bus Right[1:0] lines to enable control of an external multiplexer.

XM boards are capable of taking in the 10 MHz backplane clock and dividing it down to create the input and/or output sample clock.

To prevent potential conflicts with other vendor's implementation of PXI-specific signals, the drivers of these signals on Exacq boards default to high impedance state as required by the PXI specification. The system integrator must enable the drivers using the configuration tab in Exacq Control Center shown in Figure 3 before API calls will actually turn on the drivers.

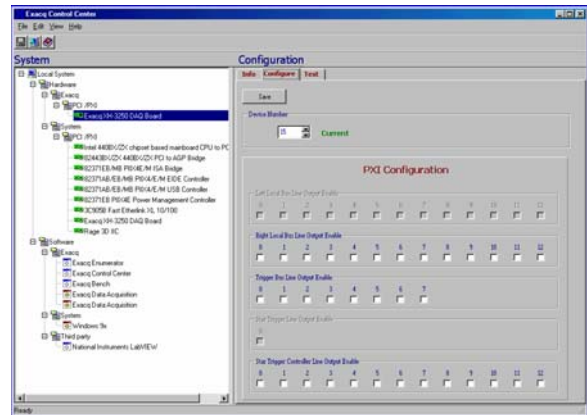


Figure 3 – Exacq Control Center PXI Tab

While this Tech Note pertains to Exacq's PXI boards, Exacq's PCI boards also feature similar functionality for multi-board synchronization, including external clock inputs and multiple triggering modes. However, the convenience of having the board to board interconnection in the PXI backplane is not available in a PCI system.

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